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EXTENDED ADDRESS DIRECT CHANNEL

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1.0 GENERAL DESCRIPTION

1.1 Scope

This document describes the performance, operation, interface, and design requirements for the Extended Address Direct Channel.

1.2 Applicable Documents

43A219604	EPS-I 655 Input/Output Multiplexer
43A219604, Appendix B	645X Input/Output Multiplexer
43A177851	EPS-I General Design Requirements for 655/355
43A236737	EPS-I 355 Direct Interface Adapter
43A177854	EPS-I MQX Board Tester
M50EB00177	Documentation Specification

1.3 Brief Description

The Extended Address Direct Channel (EADC) provides the path to interface the DATANET 355 communications subsystem to the 645X IOM via the 355 Direct Interface Adapter (DIA). (Figure 1.3) This channel may also be used to interface to the Bulk Store Controller. This EPS-I defines the requirements of the Direct Channel.

The Direct Channel will transfer data to and from the IOM central in a direct mode which will be controlled by commands received from the DIA.

Compatibility Requirements

The channel design shall be such that it will utilize existing formats and conventions so that a minimum impact will be felt in the 6000 and 355 operating systems.

Interface Requirements

The channel shall interface to the IOM central as specified in the EPS-I for the 645X IOM and the 645 IOM Design Memo 7.0.

The interface with the 355DIA is specified in Paragraph 4.2 of this EPS.

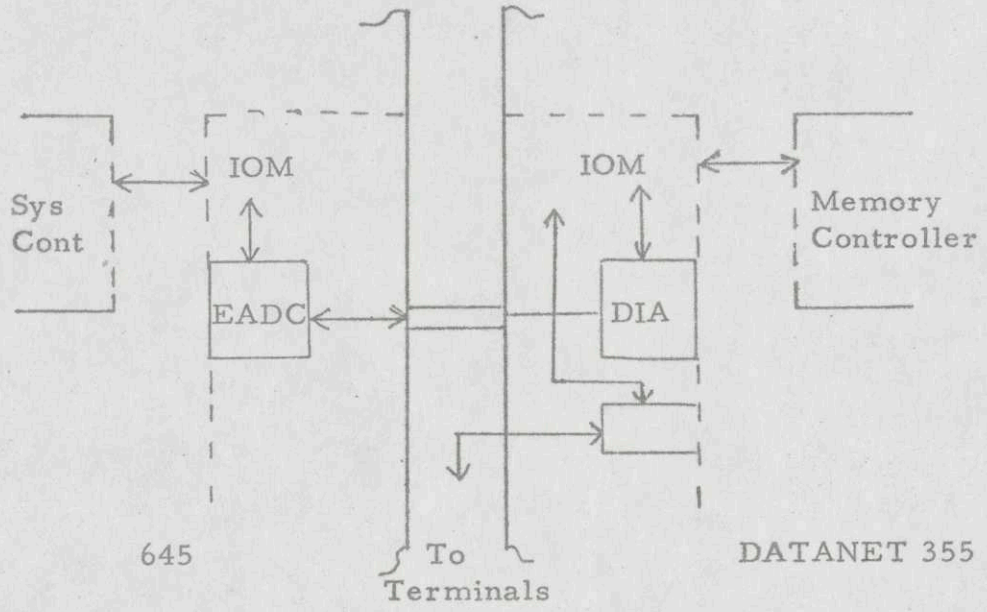


Figure 1.3

System Configuration

Packaging Requirements

The Direct Channel shall be packaged on one (1) universal board. If the channel is to be used to interface with a Bulk Store controller one (1) additional universal board will be required.

The channel shall be designed to meet the requirements of the board tester.

2.0 FUNCTIONAL CAPABILITIES

The functional capabilities are related to the Direct Channel which is to be used with the DIA. If there is any difference when the channel is used for the Bulk Store system it shall be as noted at that point.

2.1 Data Transfer Rate

The Direct Channel shall be capable of operating at speeds consistant with the DIA. This implies that the channel shall be capable of transferring 36 bit words at a rate of at least 128 KHZ.

The Bulk store channel shall transfer data in a 72 bit word (double precision). The channel shall operate at a speed consistant with the IOM data rate. This will be approximately 250 KHZ double precision words.

2.2 Buffering

The direct channel hardware is to be kept at a minimum. Therefore, the direct channel shall provide buffering only when necessary. This means that data provided to the channel from the DIA be supplied until the end of the particular memory cycle. Likewise, the channel shall present data to the DIA until a response from the DIA indicates that it has been accepted.

2.3 Error Detection

The Direct Channel shall provide the capability to check parity on data transfers. These parity checks shall be made on

a) Address and Command information from the DIA

b) Data information from the DIA

c) Data information from the IOM

The parity bit must be valid on data transfer from the DC to the IOM regardless of validity from DIA.

The channel shall present the results of these checks to the DIA. In addition, the channel shall forward to the DIA errors detected by the IOM. (Parity error on data to IOM and system faults.)

2.4 Test and Diagnostic Features

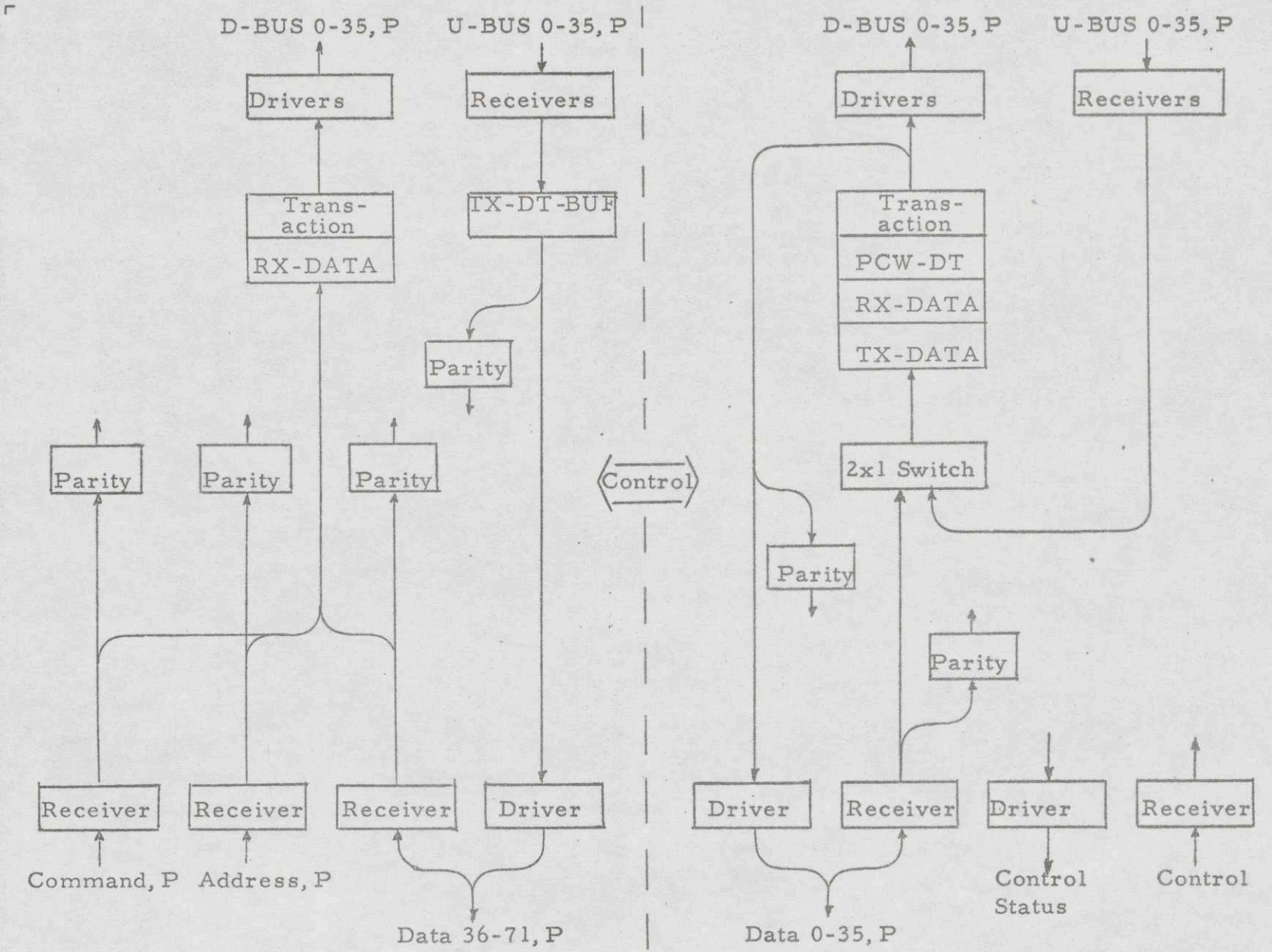
The channel shall provide T&D capabilities to test the operation of the channel as a single unit. It shall also provide the capability of being tested in conjunction with the DIA. This shall be accomplished with available circuitry after the primary functions of the channel have been completed. Paragraph 5.0 defines this criteria in more detail.

2.5 Functional Diagrams (Figure 2.5)

The diagram indicated shows a general means of implementing the required functions. It should not be construed as an attempt to present a hardware design.

Figure 2.5

Extended Address Direct Channel Functional Diagram



Bd 1 - DIA
Bd 1 & 2 - Bulk St.

3.0 DESCRIPTION OF OPERATION

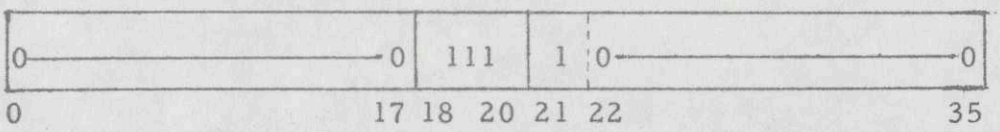
3.1 645X Connect

The 645X system software will preassign data buffer areas and generate the appropriate control words which are placed in the Direct Channel mailbox location. The system software will issue a connect to the IOM Connect Channel. The Connect Channel will obtain the Program Control Word (PCW) which will be forwarded to the Direct Channel. The Direct Channel shall respond by sending a CONNECT signal to the DIA. The DIA shall respond to this CONNECT by performing a READ/CLEAR service, via the Direct Channel, to the Direct Channel mailbox to the control word. This control word will instruct the DIA what operation is to be performed, the 645 memory address for the associated data and the interrupt cell to be set at the completion of the operation.

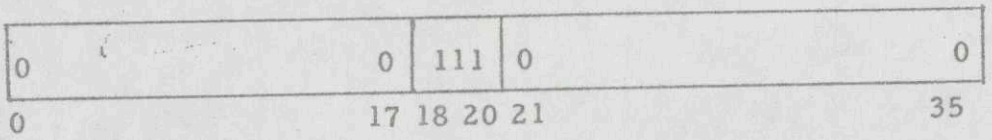
The CONNECT signal will be sent to the DIA until the RST-CON signal has been received from the DIA. The CONNECT signal may be received while the Direct Channel is in a data transfer sequence. The CONNECT signal will be sent to the DIA in the same manner specified above.

If the Direct Channel receives a system fault signal while in process of performing an IOM service, the Direct Channel will go into a MASKED state. This state will prevent the Direct Channel from initiating any IOM service request. The channel will remain in this state until the 645X software issues a PCW to unmask the channel. When the channel has entered the MASKED state because of a system fault, the system fault status will be presented to the DIA until the channel is placed into the UNMASKED state. The PCW which is unused to reset the system fault will not be forwarded to the DIA as a CONNECT signal.

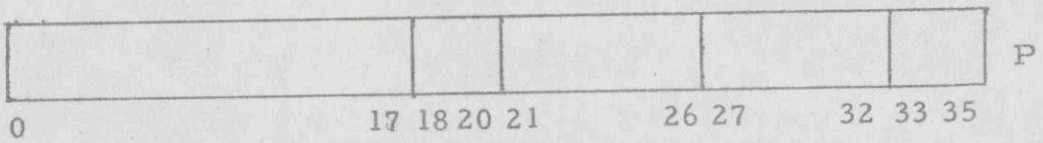
The following is the PCW-MASK format received at the Direct Channel.



The following is the PCW-unmask format received at the Direct Channel.



The following is the address/command data format used by the DIA to perform a READ/CLEAR operation to the Direct Channel mailbox location.



0-17	Direct Channel mailbox address bit 2^{17}-2^{0}.
18-20	Address extension bits 0-2 (2^{5}-2^{3}).
21-26	Must be zero, channel no. is inserted by Direct Channel.
27-32	645X IOM service code, must be 64_{8} (direct read/clear-single precision).
33-35	Address extension bits 3-5 (2^{2}-2^{0})

3.2 Data Transfer

All data transfer operations between the Direct Channel and the 645X IOM will be direct single precision services. These memory address and IOM service commands will be provided by the DIA for each service requested.

3.2.1 Data Transfer to 645X

Figure 3.2.1 shows the timing which takes place during a data transfer operation to the 645X system. This operation will consist of an address/command transfer from the DIA to the Direct Channel followed by a data transfer operation.

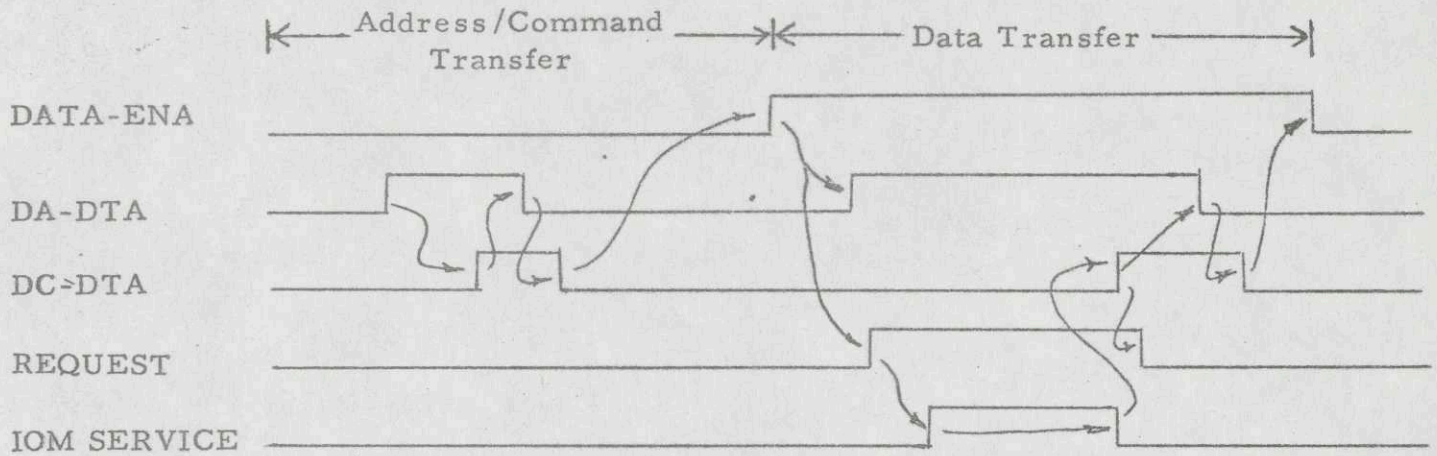
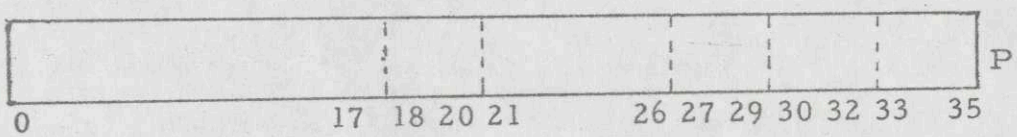


Figure 3.2.1

Data Transfer to 645X

This address/command format for the data transfer to the 645X is given below.



0-17	645X memory address 2^{17}-2^{0} to receive data
18-20	645X memory address extension 2^{5}-2^{3}
21-26	must be zero
27-32	IOM service code, must be 70_{8} (direct store-single precision)
33-35	645X memory address extension 2^{2}-2^{0}

This address/command information shall be checked for odd parity. A parity error on the address command data shall prevent the Direct Channel from accepting any IOM service request until the error condition has been cleared. This condition can only be cleared by a channel initialize signal or by a valid address command transfer. This status condition shall also be made available to the 645X system as bit 3 of the Direct Channel status word (see Paragraph).

The Direct Channel shall check odd parity on the data transferred from the DIA. If a parity error condition exists the Direct Channel shall set a status flag to indicate that fact. The Direct Channel shall also insure that the parity presented to the 645X IOM is valid (odd). At the end of the IOM service the Direct Channel will monitor the status lines from the IOM. The Direct Channel shall provide all status information to the DIA.

3.2.2 Data Transfer to 355

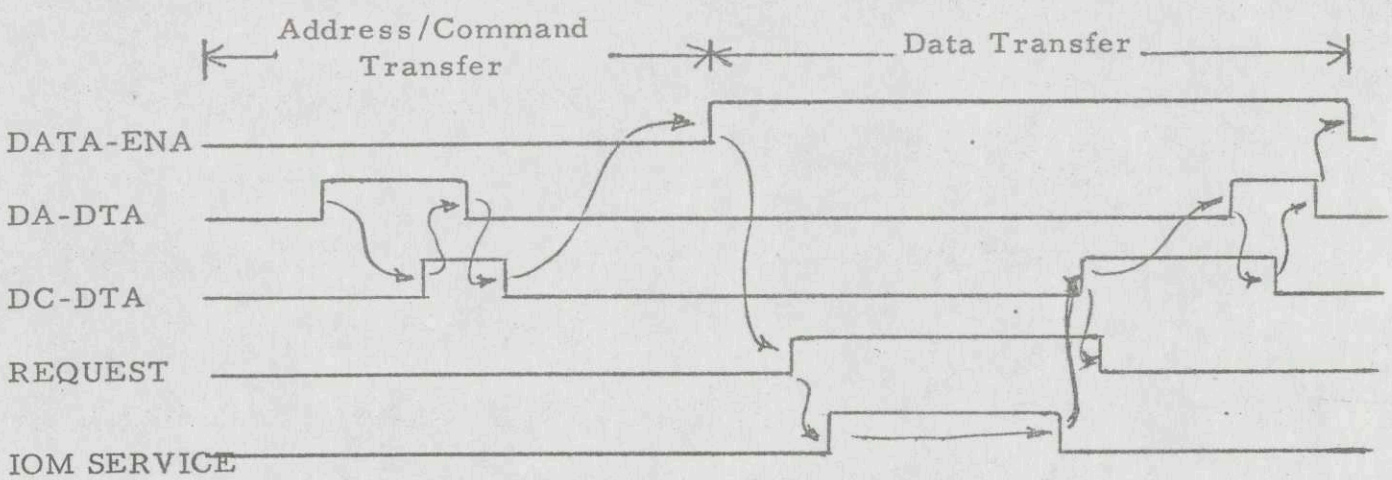
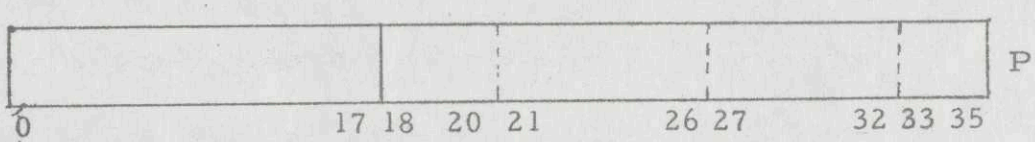


Figure 3.2.2

Data Transfer from 645X

Figure 3.2.2 shows the timing which takes place during a data transfer operation to the DATANET 355. The transfer of address/command information shall take place in the same manner stated in Paragraph 3.2.1. The format of this information is given below:

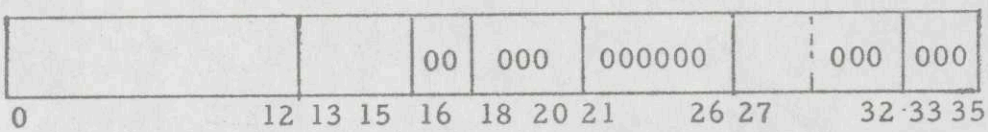


0-17	Address bits 2^{17}-2^{0} of data memory location
18-20	Address extension bits 0-2 (2^{5}-2^{3})
21-26	Must be zero, channel no. inserted by Direct Channel (direct load-single precision)
27-32	645X IOM service code, must be 60_{8}
33-35	address extension bits 3-5 (2^{2}-2^{0})

When the address/command transfer has been completed the data transfer sequence is initiated by the DIA sending the REQUEST signal. The Direct Channel shall perform the required IOM service sequence. The Direct Channel shall present the DC-DTA signal at least 50 nanoseconds after the data has been enabled to the DIA. The parity bit will be passed to the DIA as it was received from the IOM. If a parity error is detected by the Direct Channel the U-BUS-PAR-ERR status bit will indicate that fact. The Direct Channel will not change the data parity bit, i.e., it is the responsibility of the DIA to insure the proper parity.

3.3 645X Program Interrupt

The DIA may initiate a Program Interrupt (PI) service to the 645X by completing the address/command sequence and sending a REQUEST signal. The address/command format is given below.



0-12, 16-26, 30-35 must be zero

13-15 indicates interrupt level to be set which has the following meaning.

011 common peripheral - terminate interrupt
101 common peripheral - marker interrupt
111 common peripheral - special interrupt
001 IOM interrupt
000, 010, 100, 110 presently undefined

27-29 service request code, must be 011; PI service

The Direct Channel shall report the existing status to the DIA at the end of the IOM PI service. Figure 3.2.2 shows timing associated with PI service.

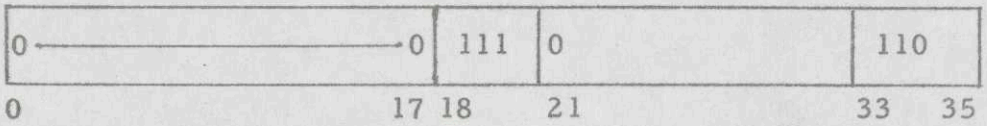
3.4 Bulk Store Controller Operation

The operation of the Bulk Store Controller with the Direct Channel will be fundamentally the same as specified above. The Bulk store controller may operate in single precision (right justified) or in double precision. The IOM service codes must be modified to include the double precision command, i.e., address/command bit 31 must be "1."

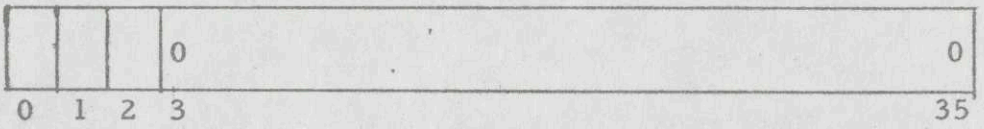
3.5 Direct Channel Status Service

Since the Direct Channel is basically a passive box there will exist conditions in which the DC/DIA subsystem is idle when it supposedly should be performing some operation. So that these conditions may be verified the Direct Channel shall have the capability of accepting a coded PCW as a request status command. The channel shall perform an indirect status service to report status. The format of the PCW and status words are given below.

Request Status PCW



Direct Channel Status Word



0	DIA power off, i.e., no operational line
1	Command parity error condition exist
2	DIA is in T&D mode
3-35	Must be zero

Word 2 is generated by IOM and has no meaning.

4.0 DIRECT CHANNEL INTERFACE

The Direct Channel will have two basic types of interfaces. The first is a high reliability level interlocked control and status interface with 37 bi-directional information lines. This interface is used when the channel is to be interfaced with a slow speed, less than 150 KHZ, system. Thus, this interface is used for the Direct Interface Adapter which is used to link the DATANET 355 to the central system. Data services with the EA-IOM will only be direct single precision. The second type of interface is a pulsed interface. This requires the Direct Channel to be configured as two boards. The channel will transfer data only in 74 bit parallel, double precision services.

4.1 645X IOM Interface

The Direct Channel will meet the EA-IOM interface specified in the 645 Follow-On Extended Address IOM Design Memo No. 7.0.

Data transfer to/from the IOM will be by direct single precision services only.

4.2 DIA Interface

4.2.1 Circuit Set

The circuits used in the Direct Channel is the NPL set consisting of line drivers (DKLD1-43C216456P1A) and line receivers (DLKR1-43C216457P1A). The intracabinet cabling is twisted pair from the channel to the EA-IOM cabinet frame. The interface cable is a 75 ohm coax cable, 43D149316. This cable length will be a minimum of fifty (50) feet and a maximum of one hundred and twenty-five (125) feet. Under no circumstances will this length be exceeded. The EA-IOM bulkhead panel will contain two connectors assemblies (connector - 43D149801P3 with insert pins 43C22904iP4). This requires that the external system use a connector assembly of 43D140801P1 with insert pins 43C229041P3.

The use of this circuit set will have an interface true logic level of +5V and a false logic level of 0V.

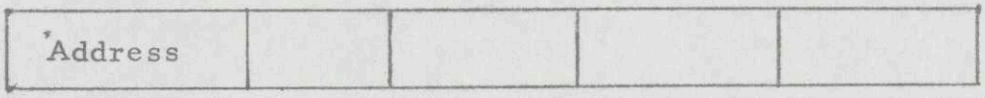
4.2.2 Information Lines

There are thirty-seven (37) bi-directional information lines (36 data + parity). The Direct Channel will keep its information line drivers disabled at all times except in response to commands from the external system. These may be a request for a read data service or a T&D command. These lines may also be used to forward commands to the external system when the Direct Channel is in the T&D mode. The parity bit is not valid when either the Direct Channel or external system is in this T&D mode.

The information presented by the external system may be an address/command information or data to be stored in the central system.

The following is the format of information received by the Direct Channel.

Address/Command for Data Transfer



0-17 Address bits (2^{17}-2^{0}) of memory locations

18-20 Memory address bits 2^{23}-2^{21}

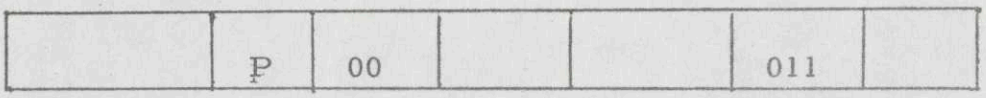
21-26 Must be zero. The Direct Channel will insert channel number in this block.

27-32 Specifies the IOM service request code. Must be one of the following

60_8 Direct Load/S.P.
64_8 Direct Read/Clear/S.P.
70_8 Direct Store/S.P.

33-35 Memory address bits (2^{20}-2^{18})

Address/Command for Program Interrupt



0-12, 16, 17, 18-26, 30-35 must be zero

13-15 Specifies which PI Cell is to be set. This code has the following meaning to the operating system.

000 undefined	100 undefined
001 IOM overhead	101 Com Per Marker
010 undefined	110 undefined
011 Com Per Terminate	111 Com Per Special

21-26 This block will be filled with Direct Channel channel number.

27-29 Must be 011. This specifies a program interrupt service to the IOM

4.2.3 Control/Status Lines

The following are the control signals which originate in the Direct Channel.

DC-OPL (Direct Channel-operational line)

This line will be high (+5V) at all times except when the Direct Channel is operating in the T&D mode. This line will also be low if the EA-IOM has lost power confidence. If this line is low (0V) the external system must disable its information line drivers.

DC-INIT (Direct Channel initialize)

This line will go high (+5V) when the Direct Channel receives an initialize signal from the EA-IOM. This line will also go high for 50 ns when the Direct Channel is in the MASK state and the channel goes into the T&D mode of operation.

DC-TEST (Direct Channel test)

This signal will go true (+5V) when the Direct Channel is in the T&D mode of operation which requires responses from the external system. This basically allows the central system T&D software to exercise the external system.

DC-DTA (Direct Channel Data)

This signal operates in conjunction with the DA-DTA signal generated by the external system.

When information is transferred from the external system to the Direct Channel the information must be transmitted fifty (50) nanoseconds prior to sending the DA-DTA signal. Thd DA-DTA indicates that the data on the Interface is valid. When the Direct Channel has accepted the data it will respond with the DC-DTA signal which in turn allows the DC-DTA signal to be removed. The status lines which are generated in the Direct Channel will be valid at the trailing edge of DC-DTA.

When information is to be transferred from the Direct Channel to the external system the data will be applied to the interface fifty (50) nanoseconds prior to the channel sending the DC-DTA signal. This signal will be transmitted until the external system responds with the DA-DTA signal. This Direct Channel status lines will be valid at the trailing edge of DC-DTA. The external system must remove the DA-DTA signal for at least two-hundred (200) nanoseconds prior to initiating a new interface transfer sequence.

CONNECT

This line will go true (+5V) when the Direct Channel receives a connect (PCW-unmasked) signal from the central system. This signal will remain true until the external system responds with the RST-CON signal. It should be noted that this CONNECT signal may go high at anytime during a data transfer sequence taking place on the DC/external system interface. The external system must remove RST-CON when it detects that the Direct Channel has removed the CONNECT signal.

The CONNECT signal is also used when the Direct Channel is operating in the external test T&D mode. In this mode it is used to indicate that there is a T&D command present on the interface. The signal will be removed when the RST-CON signal has been received. The parity information bit is not valid during this transfer.

The following are the status lines which are presented to the external system. These lines are to be considered valid ONLY at the trailing edge of DC-DTA.

CMD-PAR-ERR (Command Parity Error)

This signal indicates that a parity error has been detected on the last address/command transfer sequence. This line will remain true until a valid parity (odd) has been received during an address/command transfer. This status line is used in the Direct Channel to prevent any IOM service request from being initiated. This means that the system may be locked up because of this status condition.

This status may also be reset upon receipt of the initialize signal from the IOM.

DTA-PAR-ERR (Data Parity Error)

This line will be true (5V) when the Direct Channel has detected a parity on the data transferred from the external system. However, the parity bit will be toggled and the data will be stored in memory with correct parity. This line is to be sampled by the external system only at the trailing of DC-DTA.

U-BUS-PAR-ERR (U-Bus Parity Error)

This status line will be true when the Direct Channel has detected a parity error on data received from the EA-IOM. The parity received at the external system should be identical to that received by the Direct Channel. Thus, if this status line is true it is the reponsibility of the external system to insure proper parity. This line is valid only at the trailing edge of DC-DTA.

IOM-PAR-ERR (IOM Parity Error)

This status line will be true when the IOM has detected a parity error on the data transferred from the Direct Channel to the IOM. The IOM will correct the parity error before the data is stored in Memory. This line is valid only at the trailing of DC-DTA.

SYS-FAULT (System Fault)

This status line indicates that a system fault (memory parity error) has occurred on an IOM service requested by the Direct Channel. The Direct Channel will go into a Masked state upon detecting a system fault. This line is valid at the training edge of DC-DTA.

4.2.4 The following control lines originate in the Direct Interface Adapter.

DA-OPL (Direct Interface Adapter - operational)

This line will be a true logic level when the DIA is operational. The line will go low if the DIA is in its internal T&D mode of operation. The Direct Channel will disable its information line drivers when the DA-OPL line is low and the DA-TEST line is low.

DA-TEST (Direct Interface Adapter - Test Mode)

This line will be a true logic level when the DIA is in its T&D mode and wishes to test the DC logic. The DC will go into a masked state upon receiving the DA-Test.signal.

DATA-ENA (Data Enable)

This line is used to define the information which may be presented on the bi-directional interface lines. If this line is low (0V) the information presented to the DC will be address and command information. This line must remain low until the transfer is complete, i.e., until DC-DTA is removed by the DC. When this line is high (+5V) the information on the interface will be data.

DA-DTA (Direct Interface Adapter - Data)

This line will operate in conjunction with the DC-DTA signal. When information is being transmitted from the DIA to the DC this line will go high (+5V) at least fifty (50) nanoseconds after the data has been enabled to the interface. Its meaning is that the interface data is valid. The DC will respond with a DC-DTA signal indicating that the interface data has been accepted. The DIA will remove the DA-DTA which causes the DC-DTA signal to be removed.

When information is being transferred from the DC to the DIA the DC-DTA signal becomes the driving force. When the DIA accepts the interface data it will respond with DA-DTA which removes the DC-DTA signal.

REQUEST

This signal is used to initiate an IOM service request. The signal will remain high until the DC responds with the DC-DTA signal. If a command parity error condition exists in the DC, the REQUEST signal will not initiate an IOM service request but will be returned to the DIA as the DC-DTA signal.

RST-CON (Reset Connect)

This signal is generated by the DIA in response to the DC CONNECT signal. When true (+5V) this signal will remove the CONNECT signal from the interface. It will be removed when the DIA senses the removal of the connect signal.

When the DC is in the mode of testing the CONNECT signal indicates that there is data on the interface lines. The RST-CON will be returned to the DC when this data has been accepted by the DIA.

4.3 Bulk Store Interface

Typical Timing sequences for the bulk store interface are shown in Figure 4.3.

4.3.1 Circuit Set

The circuit set that will be used in the NPL set consisting of the DKL line receivers and line drivers. The maximum interface cable length shall be 50 feet. This cable should be a 43D140316G50 coax cable. The circuit set also forces the interface true logic level to be +5 Volts and a false logic level to be 0 Volts.

4.3.2 Information Line

There shall be seventy-four (0-35, P and 36-71, P) bi-directional information lines. These lines shall be assumed to be transferring data to the Direct Channel unless the Direct Channel is performing/completing a load from memory service.

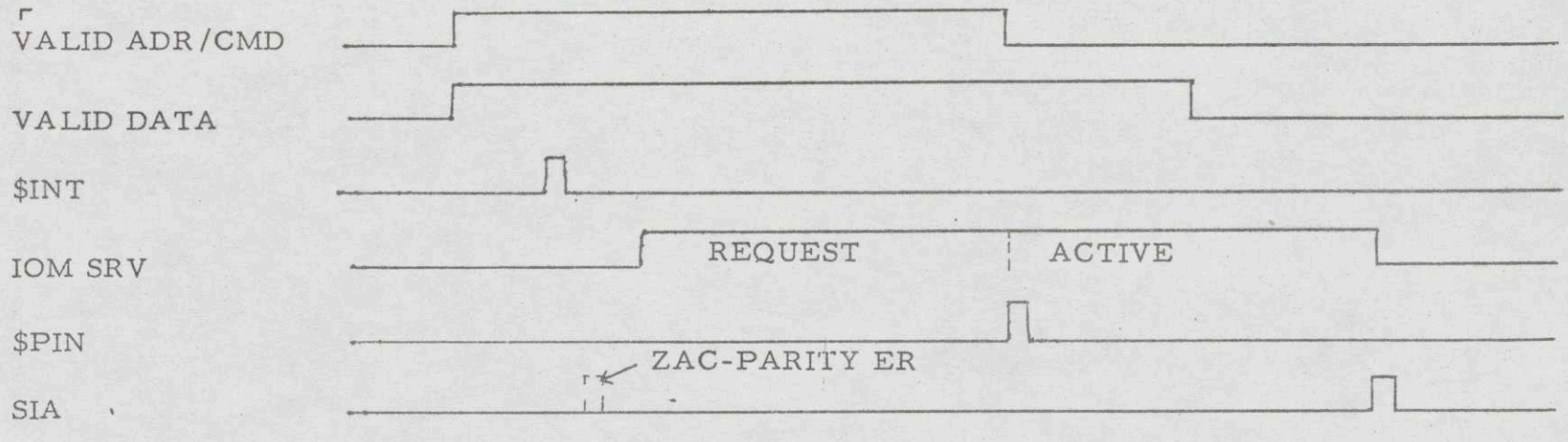
4.3.3 Direct Channel Control Signals

OPL

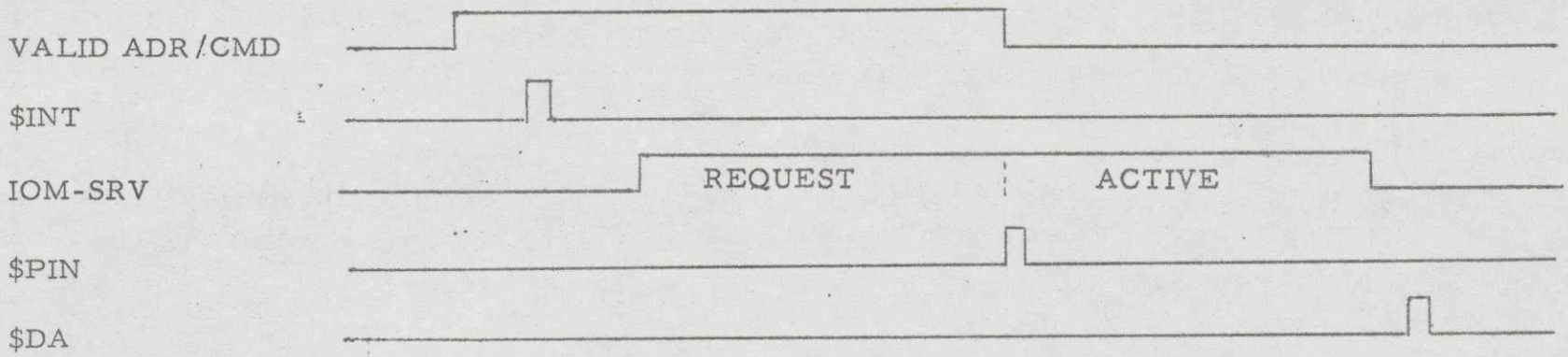
This line will be high (+5V) to indicate to the Bulk Store Controller that the Direct Channel is operational. When this line is low (0V) the bulk store controller must disable its interface line drivers. This line will go low if the IOM loses power confidence.

TEST

This line will be high (+5V) to indicate to the external system that the Direct Channel is in a T&D mode of operation which requires the participation of the external system.



Write to Memory for Bulk Store



Read from Memory for Bulk Store

Figure 4.3

Typical Bulk Store Sequences

CONNECT

This line will be high (+5V) for 100 ns when the Direct Channel has received a connect signal from the IOM.

INITIALIZE

This line will be high (+5V) when the channel receives an initialize signal from the IOM.

P-ERR-A

This line will be true (+5V) when the Direct Channel has detected a parity error on data received from the user. This line is to be sampled with the $IA pulse by the user.

P-ERR-B

This line will be true (+5V) when a parity error has been detected on the data received from the IOM. This line is to be sampled with the $IA pulse by the user.

P-ERR-C

This line will be true (+5V) when a parity error has been detected by the IOM on data transferred from the Direct Channel to the IOM. This line is to be sampled with the $IA pulse by the user.

ZAC-PAR

This line will be true (+5V) when the Direct Channel has detected a parity error on the command lines at the time the $INT signal is received. This line is to be sampled with the $IA pulse to the user.

$PIN

This line will be true (+5V) for 100 ns to indicate that the address/ command information may be changed.

$IA

This line will be true (+5V) for 100 ns to indicate that the requested service is completed. This pulse is to be used to sample the status lines and the data lines when transfer is to the user.

4.3.4 Bulk Store Control

OPL

This line will be high (+5V) when the user system is connected. The Direct Channel will provide a pull-up resistor for this line.

$INT

This line will be true (+5V) for 100 ns to indicate that the user is initiating a request for service. The address, command and data (if necessary) shall be considered valid at the time of arrival of the interrupt signal.

ADDRESS (0-23, P)

These lines will be sampled for valid parity upon receipt of the $INT signal. These lines must remain constant until the Direct Channel has responded with $PIN.

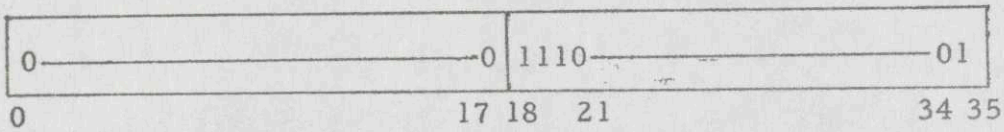
COMMAND (A, B, C, D, E, P)

These lines will be sampled for valid parity upon receipt of the $INT signal. These lines must remain constant until the Direct Channel has responded with $PIN.

5.0 TEST & DIAGNOSTICS

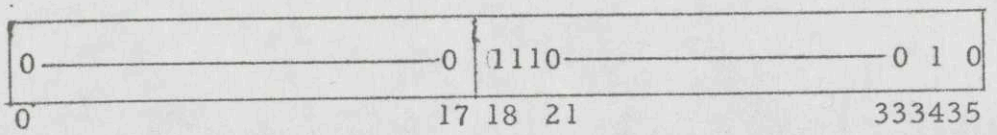
The Direct Channel shall be capable of operating in a mode which will allow software to perform T&D functions on the channel. There will be three distinct subsets of this T&D mode.

The first shall be an internal mode of operation which allows (645 resident T&D software to perform) verification of data paths and the IOM interface sequences. This mode will be entered when the channel receives a PCW with the following format.

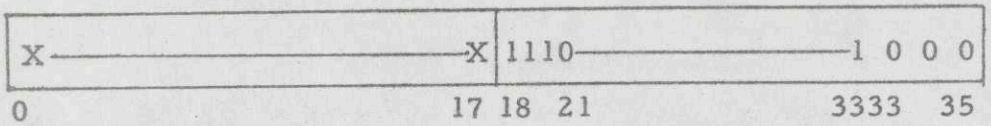


The format for the subsequent coded PCW will be dictated by hardware design so as to have a minimum effect on total hardware and allow maximum visability into the channel.

The second area of T&D shall be an external mode. This will allow 645 resident T&D software to verify operation of the DC/DIA interface and the basic data paths within the DIA. This mode is entered upon receipt of the following PCW.



The commands which are transferred to the DIA will be embedded in the following PCW.



0-17 These bits will contain the command to be transferred to the DIA. The specific codes will be specified by hardware constraints during the design phase of the DIA.

The third area is similar to the second, i.e., it will allow the DATANET 355 T&D software to verify the DC/DIA interface and data paths internal to the Direct Channel. The Direct Channel shall prevent any IOM service request from being initiated in this mode.

The above requirements shall be incorporated on a design/circuit availability basis while maintaining the one board channel configuration.

The internal T&D mode shall be available for the Bulk Store Direct Channel while the other two modes are not required.

6.0 GENERAL DESIGN REQUIREMENTS

The DC shall be designed to conform to 43A177851, General Design Requirements for GE-655/GE-635 Systems.

Wherever possible the DC shall conform to available group standards. The following is a partial list of group standards (in draft form):

- B01.08 Environment
- B01.09 General Product Safety
- B01.10 Equipment Handling, Transportation, & Storage Criteria
- B01.48 Primary Power
- B01.49 Glossary, General Design Standards

6.1 U. L. Requirements

It is mandatory that the DC be designed to conform to the requirements of U. L. Listing, U. L. 478 "Standards for Safety, Electronic Data Processing Units and Systems".

6.2 DC Circuit Technology

The DC proper shall be constructed using MQX Technology and integrated circuits. MQX logic boards shall be laid out in a manner which enables T&D programs to isolate a chip failure to one board. In addition, board design must permit chip feature isolation to the level specified by the MQX board Tester EPS-I, Drawing Number 43A177854.

6.3 Document Standards

Documentation shall conform to the standards of specification M50EB00177.